Abstract

The channel bank architecture of the present invention reduces connector density, reduces costs and other bulk components, and improves the system noise performance. The connector density is reduced through an architecture that digitizes the entire upstream spectrum and buses the digitized result to the input of multiple digital receivers. The digital receivers have all digital hardware-based filters and demodulators. Stored prototype D.C. coefficients are bandpass transformed, enabling the receivers to be programmed to essentially any arbitrary center frequency over a wide-range of bandwidths, and provide great frequency agility. Reprovisioning is possible by sending commands to the line card. The number of receiver inputs, associated connectors, and associated splitter taps is reduced by a factor of 1/M. In an illustrative embodiment, M is 16. Taking into account the total number of connectors for both upstream and downstream connectors, the connector count is reduced by a factor 1/T, where T is a function of the D/U ratio and M. In an illustrative embodiment T is 4. In an illustrative 4D x 16U CMTS channel bank embodiment, having 4 downstream channels and 16 upstream channels, four connectors are required for the downstream channels and only a single connector is required for all 16 upstream channels. The illustrative embodiment thus has 5 total connectors, compared to 20 total connectors in a comparable prior art system.